

The Definitive Guide to SystemC

David C Black, Doulos

Presented to UT Austin class: EE382N.23
Embedded System Design and Modeling
UT Austin



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The SystemC Language



- ➡ • Introduction to SystemC
 - Overview and background
 - Central concepts
 - The SystemC World
 - Use cases and benefits
- [Core Concepts and Syntax](#)
- [Bus Modeling](#)

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2

What is SystemC?

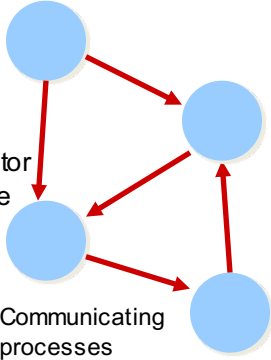


System-level modeling language

- Network of communicating processes (c.f. HDL)
- Supports heterogeneous models-of-computation
- Models hardware and software

C++ class library

- Open source proof-of-concept simulator
- Owned by Accellera Systems Initiative



Communicating processes

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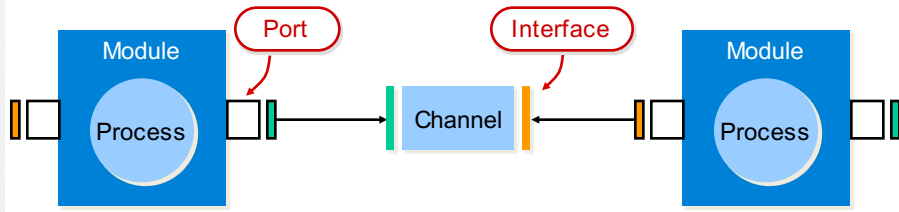
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Features of SystemC

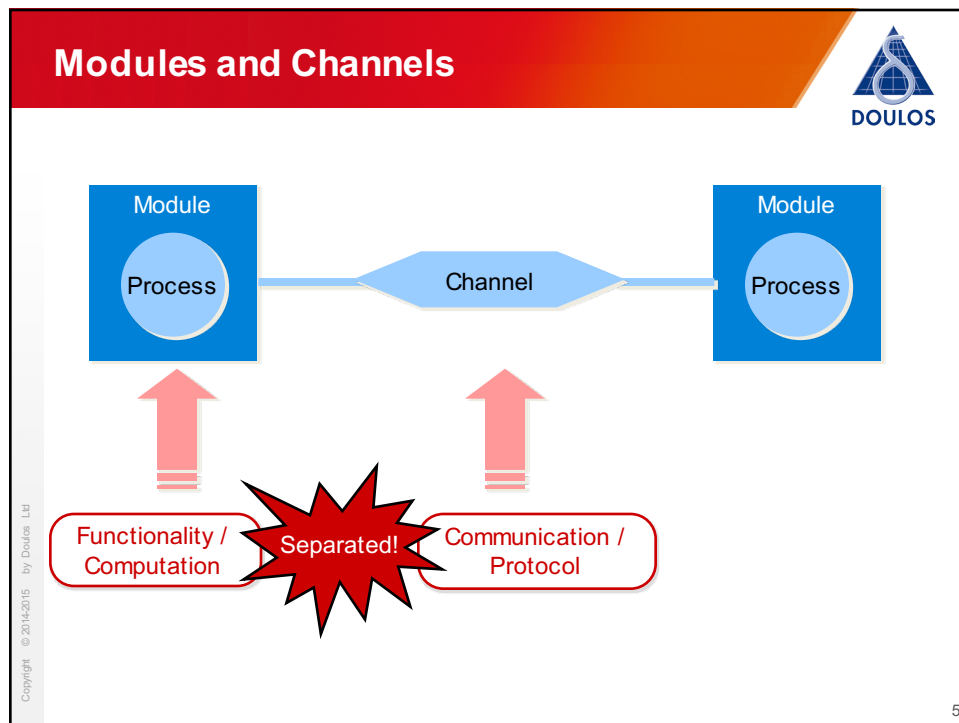


- Modules (structure)
- Ports (structure)
- Processes (computation, concurrency)
- Channels (communication)
- Interfaces (communication refinement)
- Events (time, scheduling, synchronization)
- Data types (hardware, fixed point)

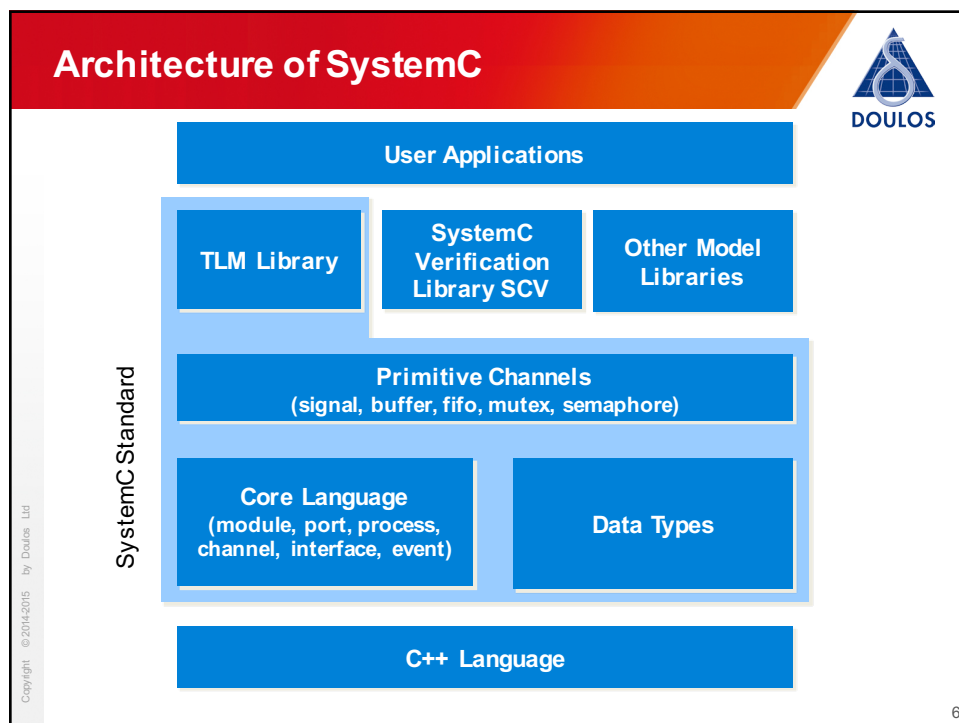


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Accellera Systems Initiative



Formed from Open-SystemC Initiative (OSCI) and Acœllera
Website <http://www.accellera.org/community/systemc>

National Users Groups

- <http://www.ti.informatik.uni-tuebingen.de/~systemc>
- <http://www.nascug.org>
- <http://www.iscug.in>
- Others...

Language Working Group LWG

- IEEE 1666™ -2005
 - SystemC 2.2 released Mar 2006 (IEEE 1666 compliant)
- IEEE 1666™ -2011
 - SystemC 2.3.1 released Apr 2014 (IEEE 1666 compliant)
 - Includes TLM-2

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Other Working Groups



Verification Working Group VWG

- SystemC Verification (SCV) library released 2003

Synthesis Working Group SWG

- Synthesisable subset of SystemC

Transaction-Level Modeling Working Group TLMWG

- TLM-1.0 released May 2005
- TLM-2.0 released June 2008
- TLM-2.0 part of IEEE 1666-2011

Analog and Mixed Signal Working Group AMSWG

Control, Configuration & Inspection Working Group CCIWG

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8

What can you do with SystemC?



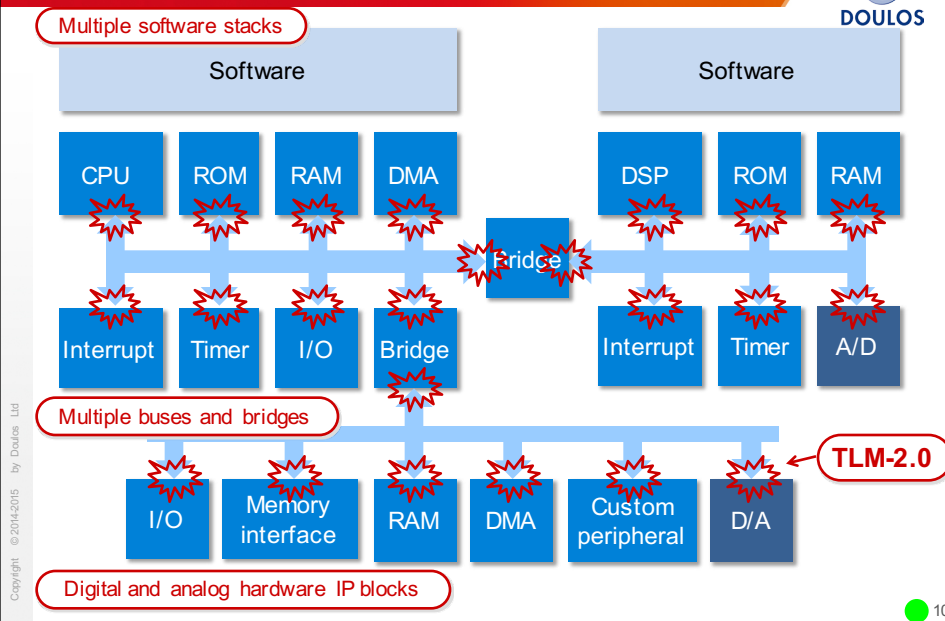
- Discrete Event Simulation (events, time)
- Register Transfer Level (delta delays, bus resolution)
 - Transaction Level (communication using function calls)
 - Kahn Process Networks (infinite fifos, reads block when empty)
 - Dataflow (input-execution-output stages)
 - CSP (rendezvous, blocking reads & writes)
- Continuous Time or Frequency Domain (Analog)
SystemC AMS
- NOT gate level
- NOT abstract RTOS modeling (process scheduling, priorities, pre-emption)
(originally planned as version 3)

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Typical Use Case: Virtual Platform



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What is SystemC Used For?



- Virtual Platform
 - Architectural exploration, performance modeling
 - Software development
 - Reference model for functional verification
 - Available before RTL - **early!**
 - Simulates much faster than RTL - **fast!**
- High-level synthesis
- Used by
 - Architects, software, hardware, and verification engineers

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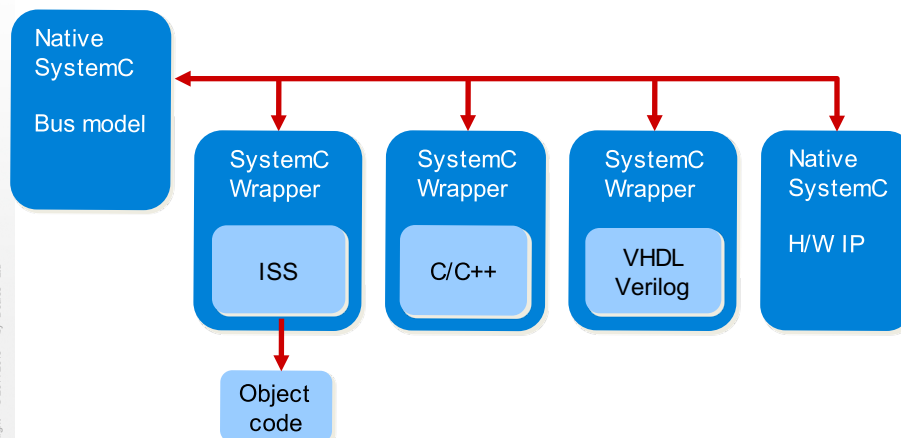
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SystemC is Glue!



- Transaction-level modeling is communication-centric



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12

Why SystemC in Particular?



- Industry standard IEEE 1666™
- Open-source C++ simulator
 - Available across multiple platforms (Linux, Windows, Mac)
 - No vendor lock-in, no licensing issues
- Easy integration with the C/C++ world
- Easy to put SystemC wrappers around existing HDL or C models
- Wide availability of tools, models and know-how
- Mature tool vendor support for co-simulation and debug

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SystemC Data Types



In namespace `sc_dt::`

Template	Base class	Description
<code>sc_int<W></code>	<code>sc_int_base</code>	Signed integer, $W < 65$
<code>sc_uint<W></code>	<code>sc_uint_base</code>	Unsigned integer, $W < 65$
<code>sc_bigint<W></code>	<code>sc_signed</code>	Arbitrary precision signed integer
<code>sc_bignint<W></code>	<code>sc_unsigned</code>	Arbitrary precision unsigned integer
		(intermediate results unbounded)
<code>sc_logic</code>		4-valued logic: '0' '1' 'X' 'Z'
<code>sc_bv<W></code>	<code>sc_bv_base</code>	Bool vector
<code>sc_lv<W></code>	<code>sc_lv_base</code>	Logic vector
<code>sc_fixed<></code>	<code>sc_fix</code>	Signed fixed point number
<code>sc_ufixed<></code>	<code>sc_ufix</code>	Unsigned fixed point number

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14

Data Type Characteristics



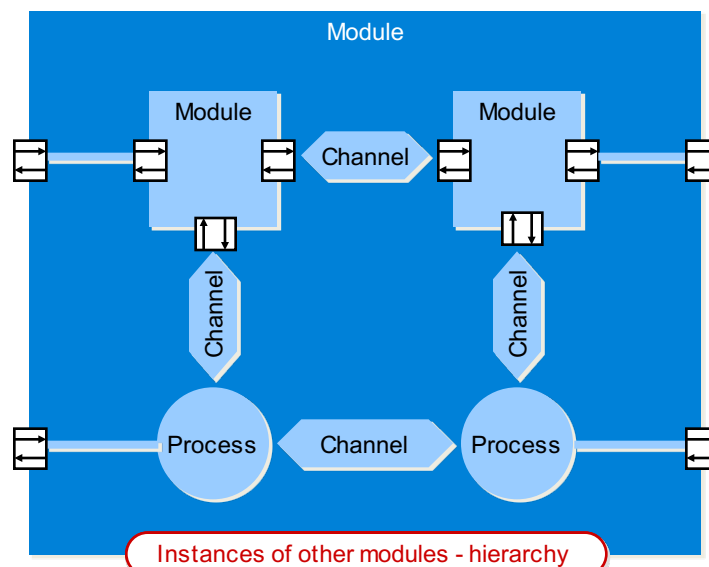
	C++	SystemC	SystemC	SystemC
Unsigned	unsigned int	sc_bv, sc_lv	sc_uint	sc_biguint
Signed	int		sc_int	sc_bigint
Precision	Host-dependent	Limited precision	Limited precision	Unlimited precision
Operators	C++ operators	No arithmetic operators	Full set of operators	Full set of operators
Speed	Fastest	Faster	Slower	Slowest

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Modules



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Example: Simple Multiplier



Class →

```
// mult.h
#include <systemc>

SC_MODULE (Mult)
{
  sc_in<int> a;
  sc_in<int> b;
  sc_out<int> f;

  SC_CTOR (Mult);

  void action();
};
```

Ports →

Constructor →

Process →

```
// mult.cpp
#include "mult.h"
using namespace sc_core;

Mult::Mult
( sc_module_name nm )
: sc_module( nm )
{
  SC_HAS_PROCESS (Mult);
  SC_METHOD (action);
  sensitive << a << b;
}

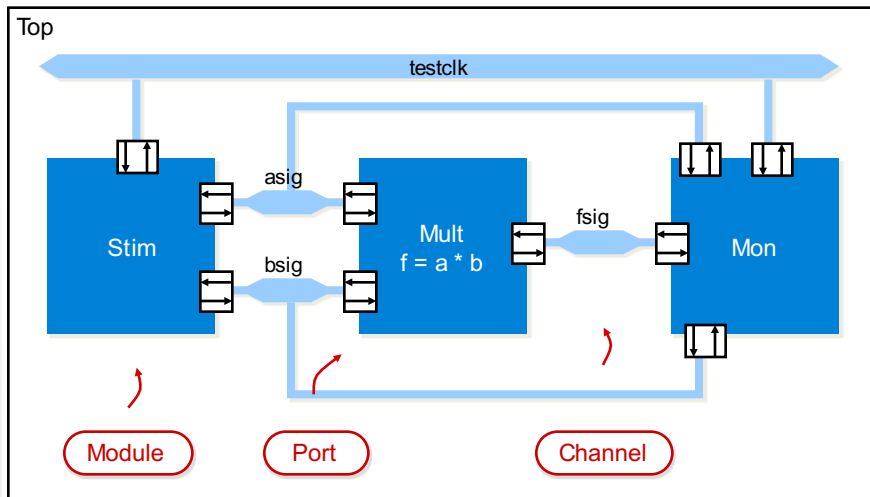
void Mult::action(void)
{
  f = a * b;
}
```

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The Test Bench



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Module Instantiation



Channels

Modules

```

SC_MODULE (Top)
{
    sc_signal<int> asig, bsig, fsig;
    sc_clock testclk;

    Stim stim1;
    Mult uut;
    Mon mon1;

    SC_CTOR (Top)
    : testclk("testclk", 10, SC_NS),
      stim1("stim1"), uut("uut"), mon1("mon1")
    {
        ...
    }
}
        
```

String name of instance (constructor argument)

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Port Binding



Alternative function

Port name

Channel name

```

...

stim1.a(asig);
stim1.b(bsig);
stim1.clk(testclk);

uut.a(asig);
uut.b(bsig);
uut.f(fsig);

mon1.a.bind(asig);
mon1.b.bind(bsig);
mon1.f.bind(fsig);
mon1.clk.bind(testclk);
}
};
        
```

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sc_main



- sc_main is the entry point to a SystemC application

```
#include "systemc.h"
#include "top.h"

int sc_main(int argc, char* argv[])
{
    Top top("top");
    sc_start();
    return 0;
}
```

Called from main()

Instantiate one top-level module

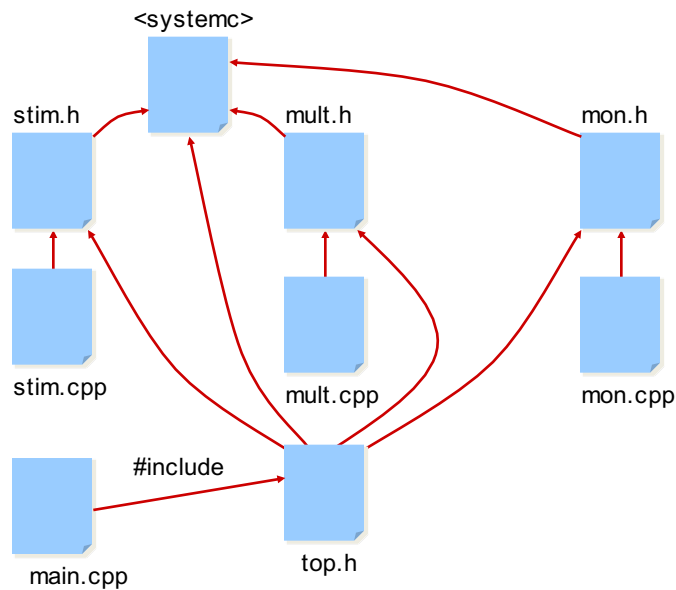
End elaboration, run simulation

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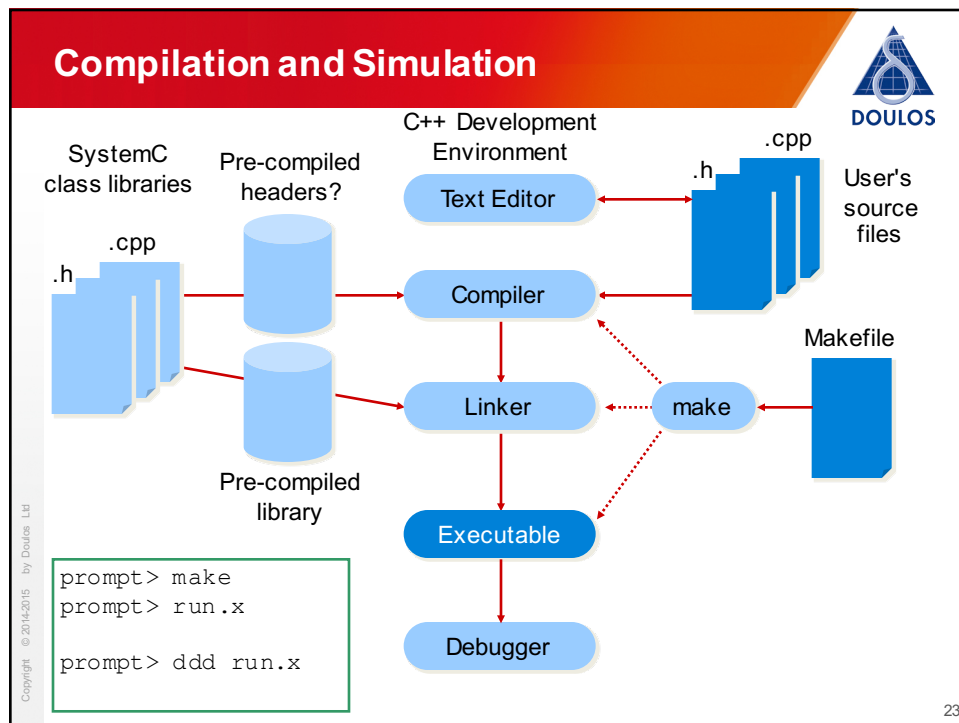
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Summary of Files

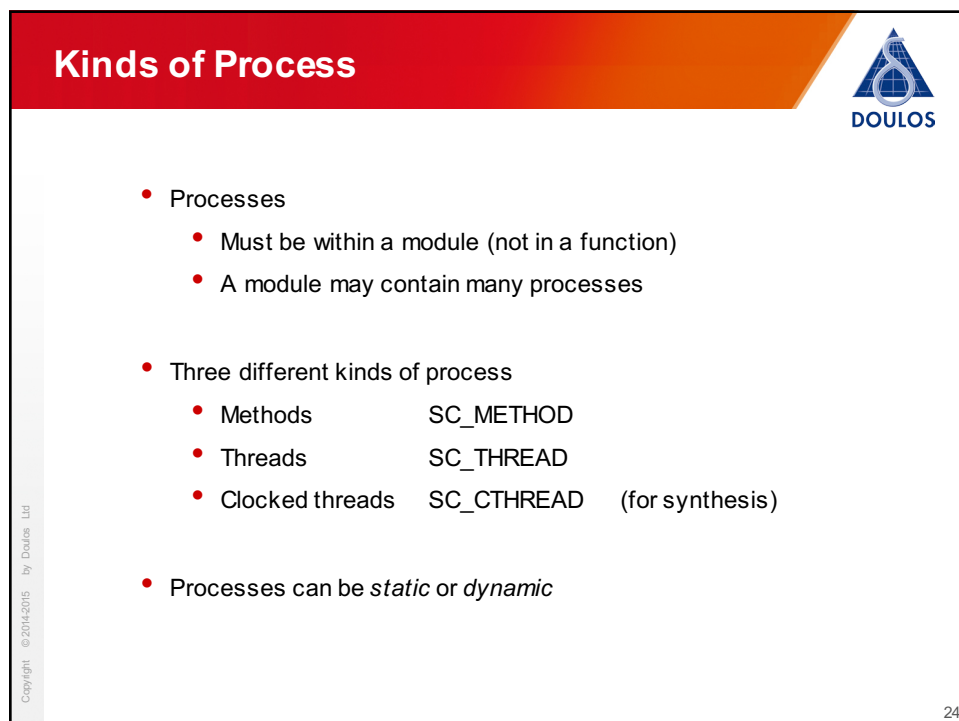


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Dynamic Sensitivity



```

SC_CTOR(Module)
{
    SC_THREAD(thread);
    sensitive << a << b;
}

void thread()
{
    for (;;)
    {
        wait();
        ...
        wait(10, SC_NS);
        ...
        wait(e);
        ...
    }
}

```

Static sensitivity list

Wait for event on *a* or *b*

Wait for 10ns

Wait for event *e*

ignore *a* or *b*

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sc_event and Synchronization



```

SC_MODULE(Test)
{
    int data;
    sc_event e;
    SC_CTOR(Test)
    {
        SC_THREAD(producer);
        SC_THREAD(consumer);
    }
    void producer()
    {
        wait(1, SC_NS);
        for (data = 0; data < 10; data++) {
            e.notify();
            wait(1, SC_NS);
        }
    }
    void consumer()
    {
        for (;;) {
            wait(e);
            cout << "Received " << data << endl;
        }
    }
};

```

Shared variable

Primitive synchronization object

Schedule event immediately

Resume when event occurs

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26

sc_time



- Simulation time is a 64-bit unsigned integer
- Time resolution is programmable - must be power of 10 x fs
- Resolution can be set once only, before use and before simulation
- Default time resolution is 1 ps

```
enum sc_time_unit {SC_FS, SC_PS, SC_NS, SC_US, SC_MS, SC_SEC};
```

```
sc_time(double, sc_time_unit);
```

Constructor

```
void sc_set_time_resolution(double, sc_time_unit);
sc_time sc_get_time_resolution();
```

```
const sc_time& sc_time_stamp();
```

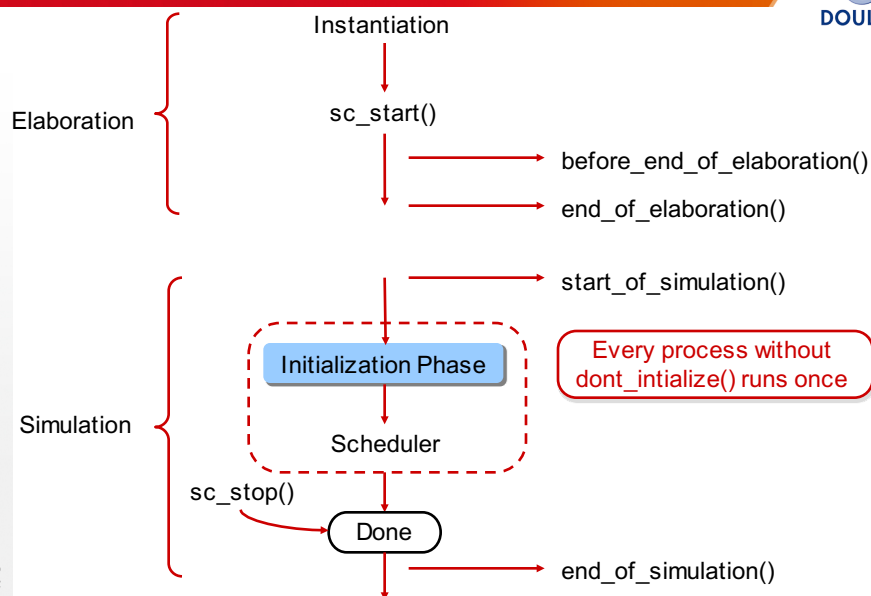
Get current simulation time

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27

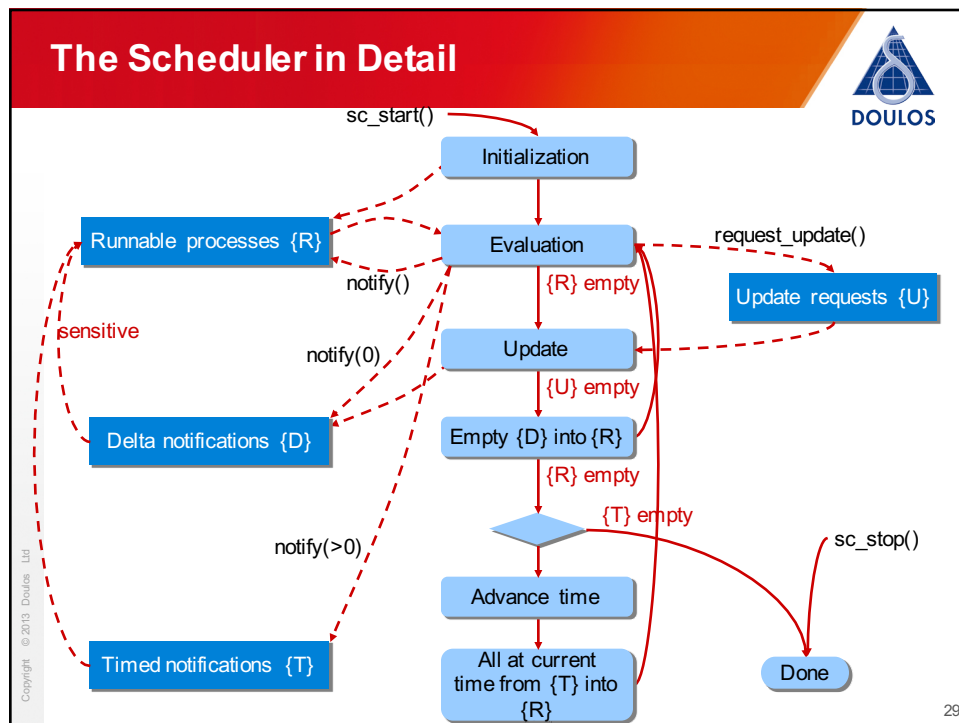
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Elaboration / Simulation Callbacks

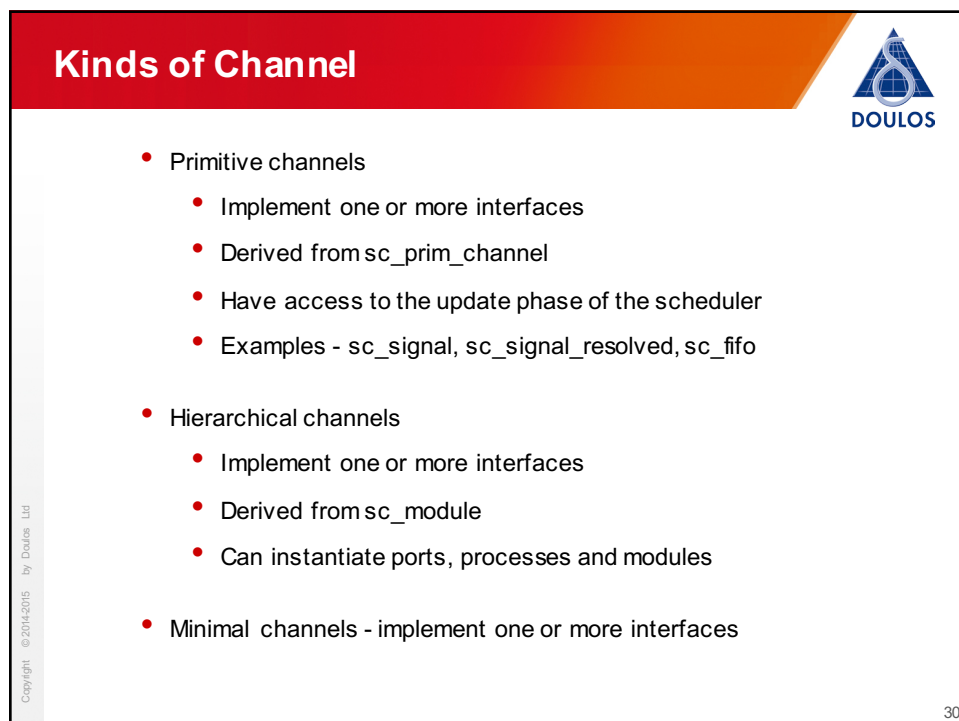


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28



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Built-in Primitive Channels



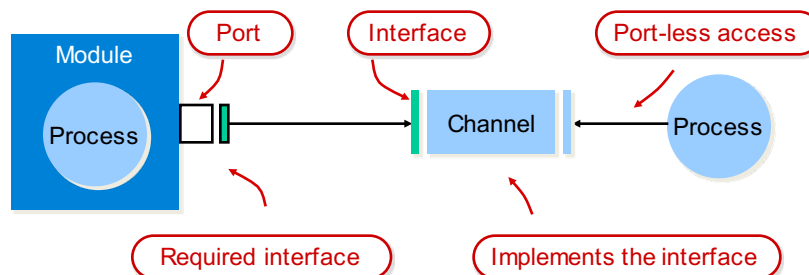
Channel	Interfaces	Events
sc_signal<T>	sc_signal_in_if<T> sc_signal_inout_if<T>	value_changed_event()
sc_buffer<T>	Same as sc_signal	On every write()
sc_signal_resolved sc_signal_rv<W>	Same as sc_signal<sc_logic>	Same as sc_signal
sc_clock	Same as sc_signal<bool>	posedge & negedge
sc_fifo<T>	sc_fifo_in_if<T> sc_fifo_out_if<T>	data_written_event() data_read_event()
sc_mutex	sc_mutex_if	n/a
sc_semaphore	sc_semaphore_if	n/a
sc_event_queue	n/a	Every notify() invocation

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31

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Interface Method Call



- An interface declares a set of methods (pure virtual functions)
- An interface is an abstract base class of the channel
- A channel *implements* one or more interfaces (c.f. Java)
- A module calls interface methods via a port

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Declare the Interface



Important

```
#include "systemc"
class queue_if : virtual public sc_core::sc_interface
{
public:
    virtual void put(char c) = 0;
    virtual char get(void) = 0;
};
```

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33

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Queue Channel Implementation



```
#include "queue_if.h"
class Queue : public queue_if, public sc_core::sc_object
{
public:
    Queue(char* nm, int _sz)
        : sc_core::sc_object(nm), sz(_sz)
    { data = new char[sz]; w = r = n = 0; }

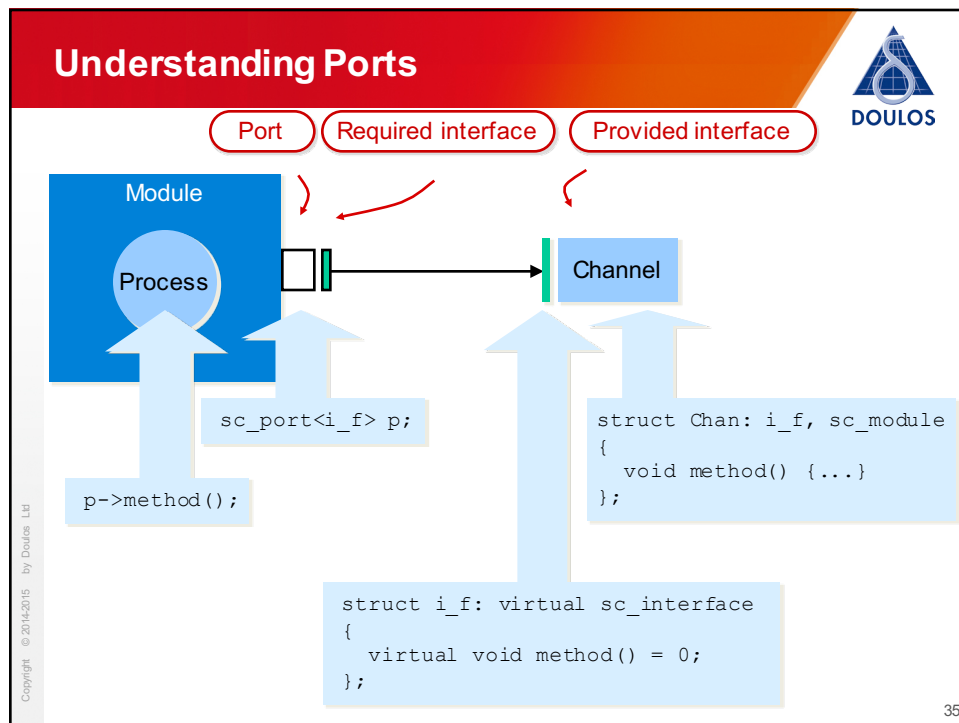
    void put(char c);
    char get(void);

private:
    char* data;
    int sz, w, r, n;
};
```

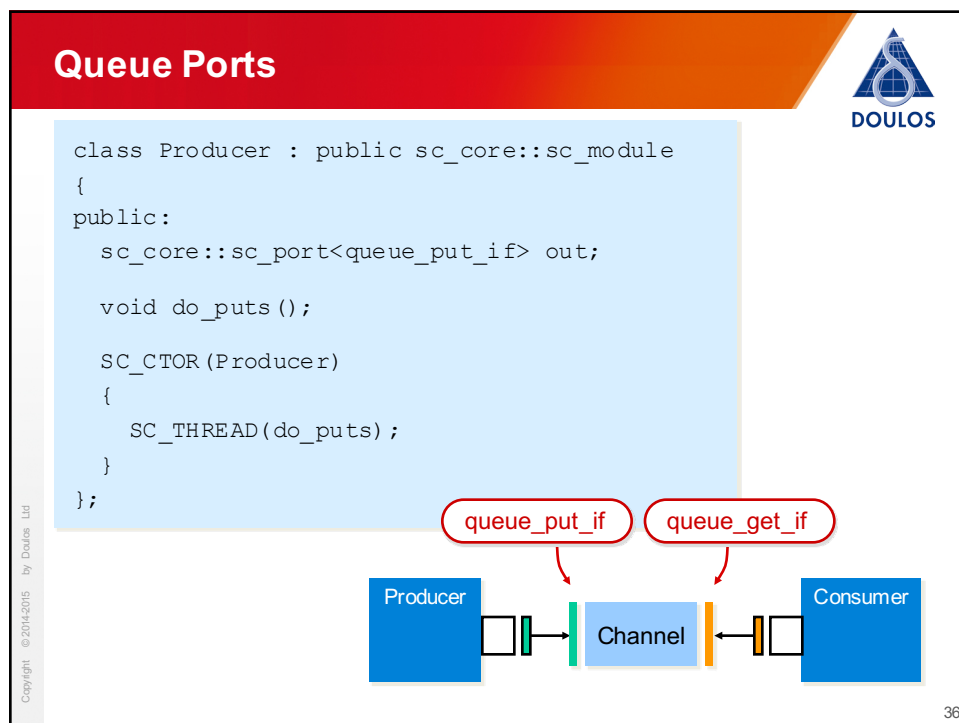
} Implements interface methods

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34



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Calling Methods via Ports



```
#include <systemc>
#include "producer.h"
using namespace sc_core;

void Producer::do_puts ()
{
    std::string txt = "Hello World.";
    for (int i = 0; i < txt.size(); i++)
    {
        wait(SC_ZERO_TIME);

        out->put(txt[i]);
    }
}
```

Note: -> overloaded

Interface Method Call

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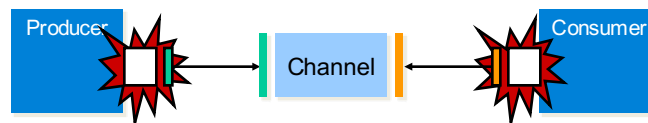
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Why Ports?

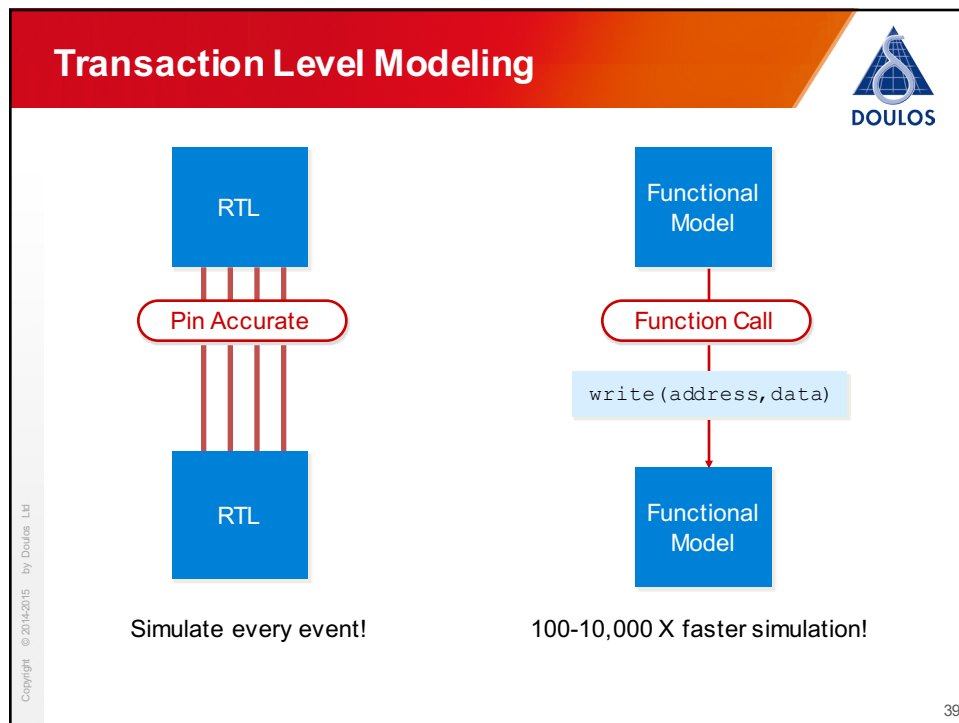


- Ports allow modules to be independent of their environment
- Ports support elaboration-time checks (register_port, end_of_elaboration)
- Ports can have data members and member functions

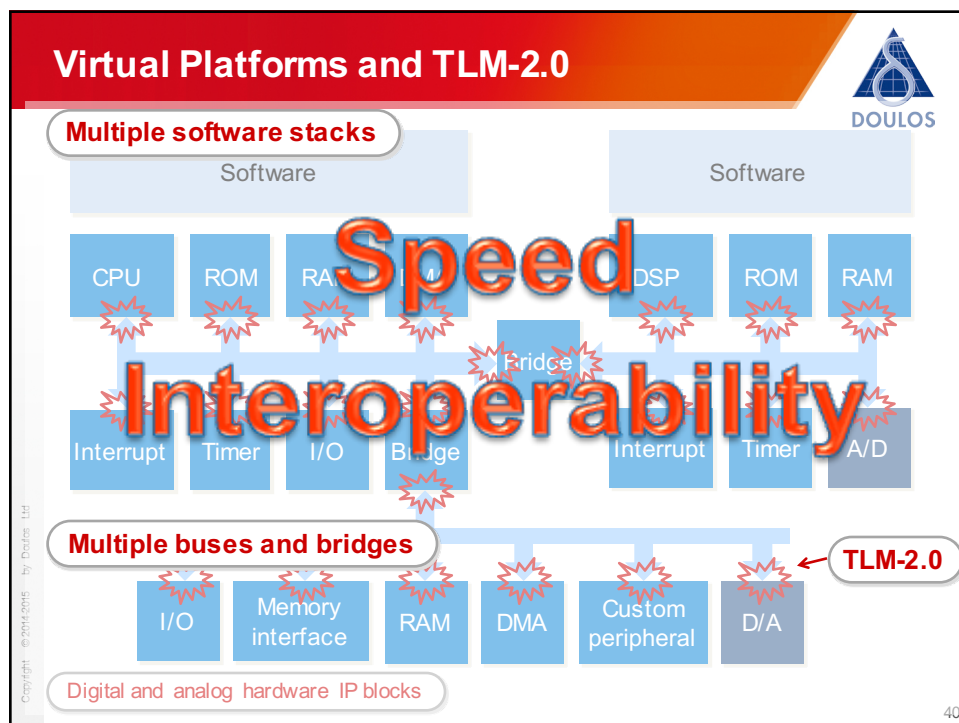


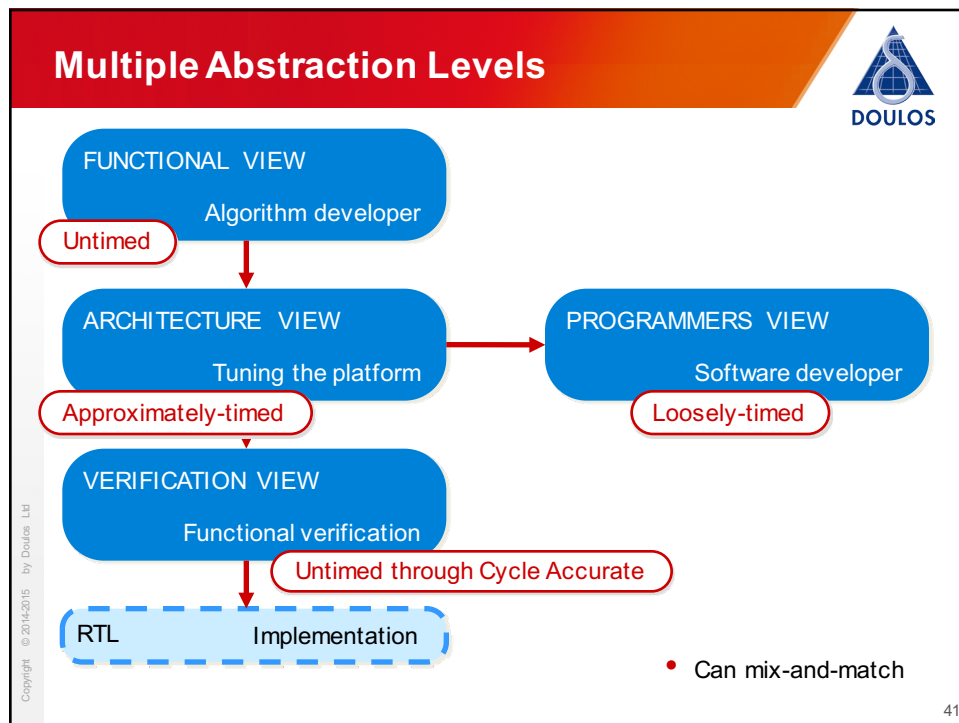
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38

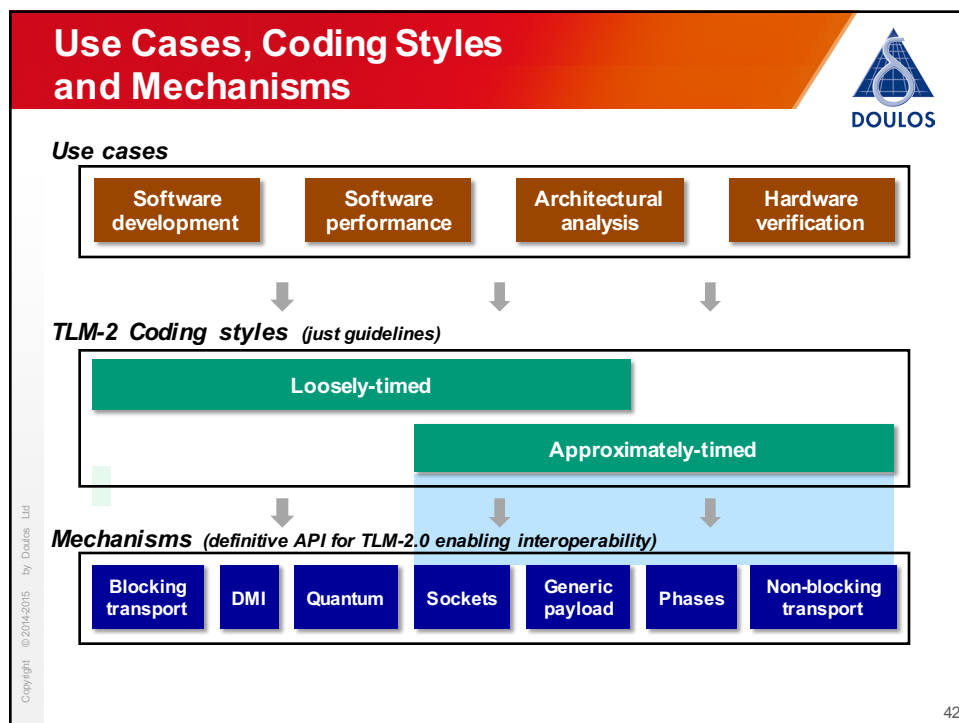


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Coding Styles



Loosely-timed = as fast as possible

- Register-accurate
- Only sufficient timing detail to boot O/S and run multi-core systems
- b_transport – each transaction completes in one function call
- Temporal decoupling
- Direct memory interface (DMI)

Approximately-timed = just accurate enough for performance modeling

- *aka* cycle-approximate or cycle-count-accurate
- Sufficient for architectural exploration
- nb_transport – each transaction has 4 timing points (extensible)

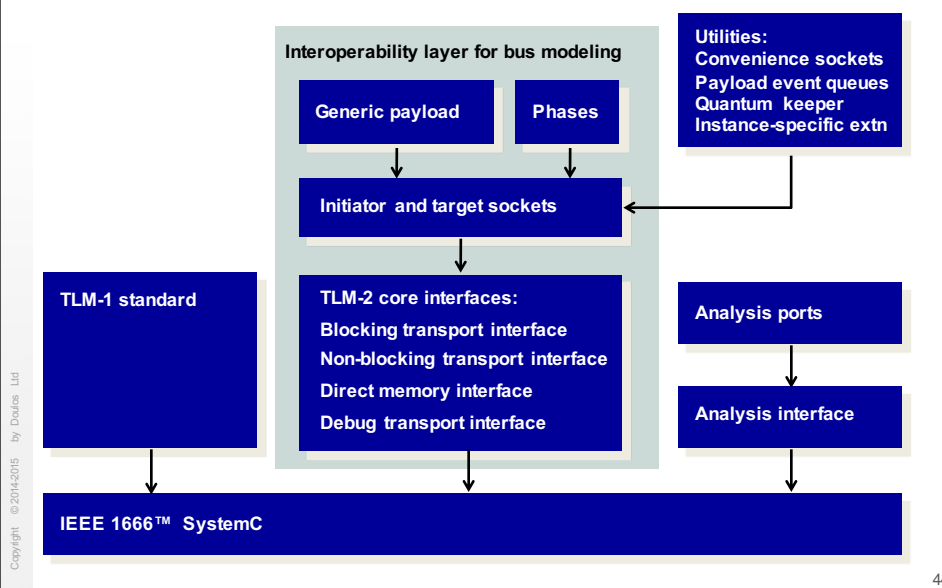
Guidelines only – not definitive

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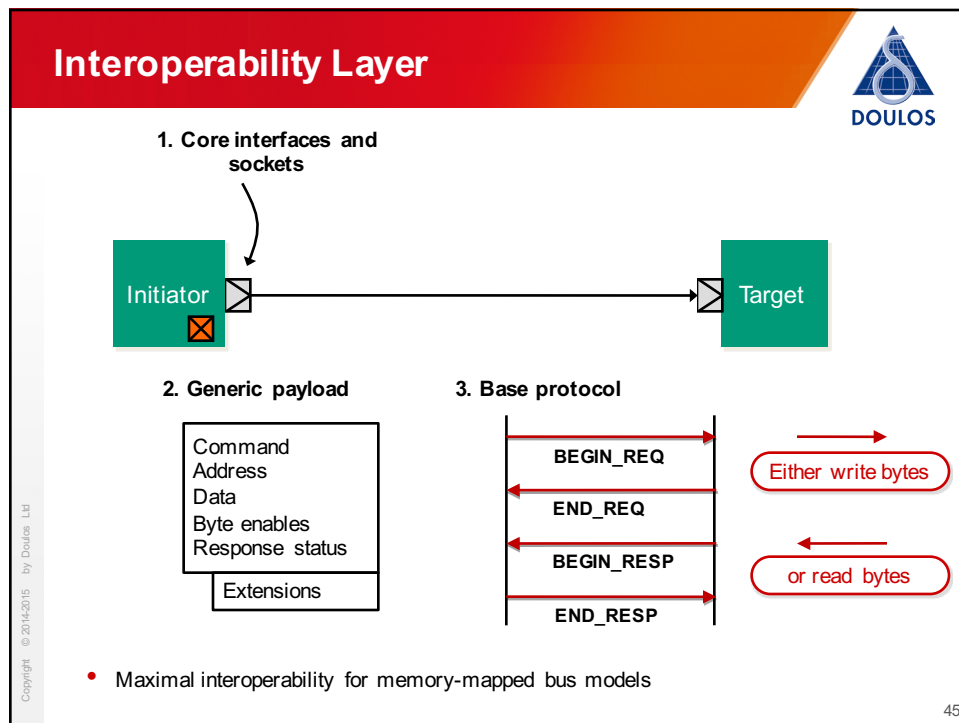
43

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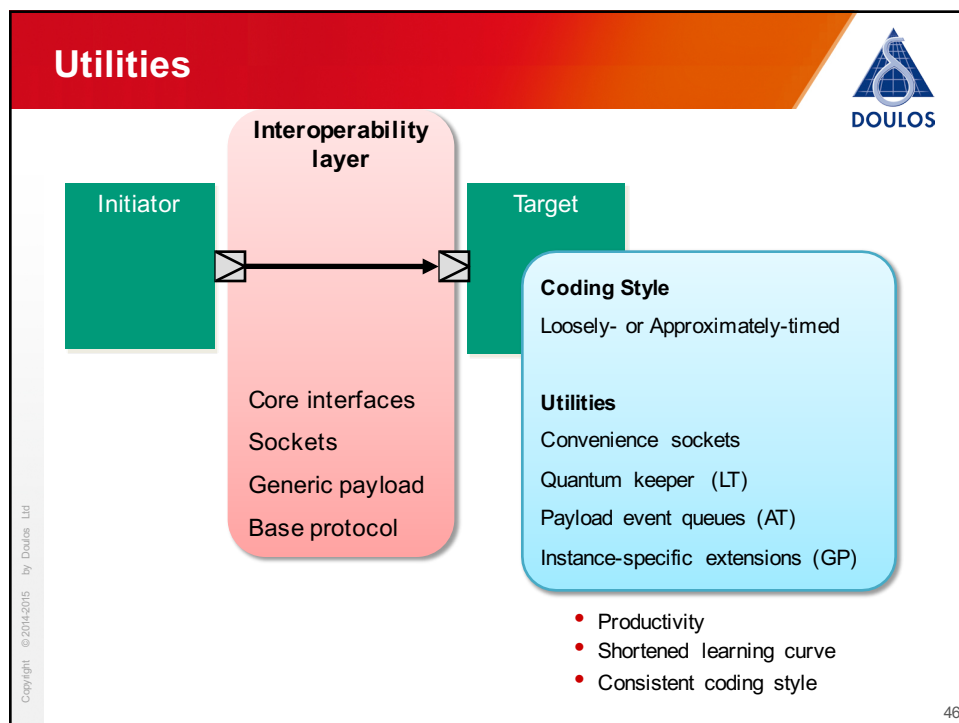
The TLM 2.0 Classes

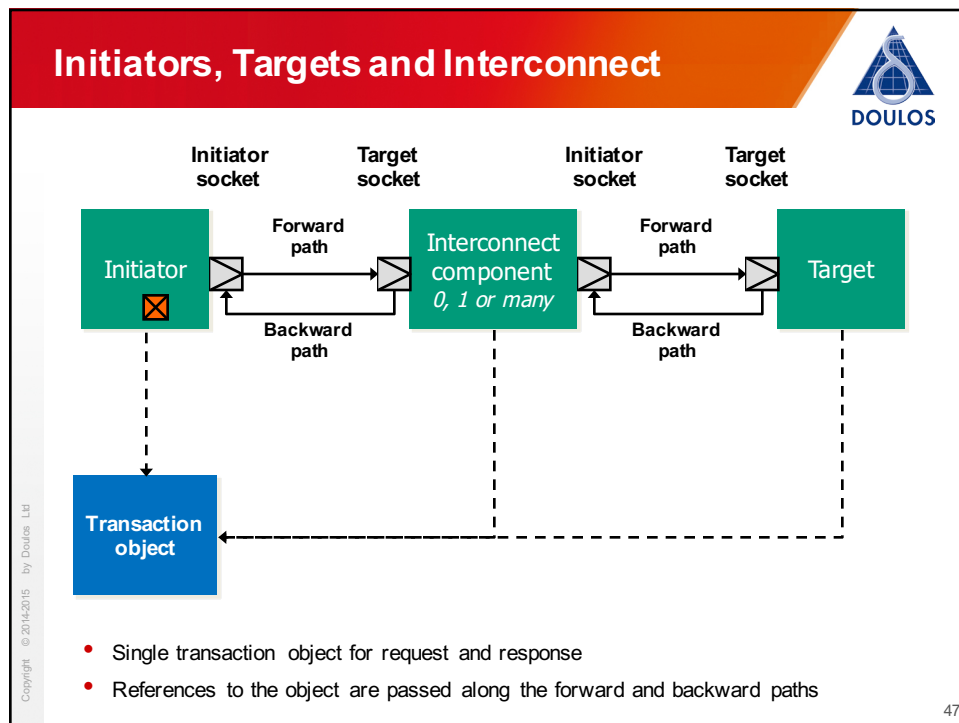


44

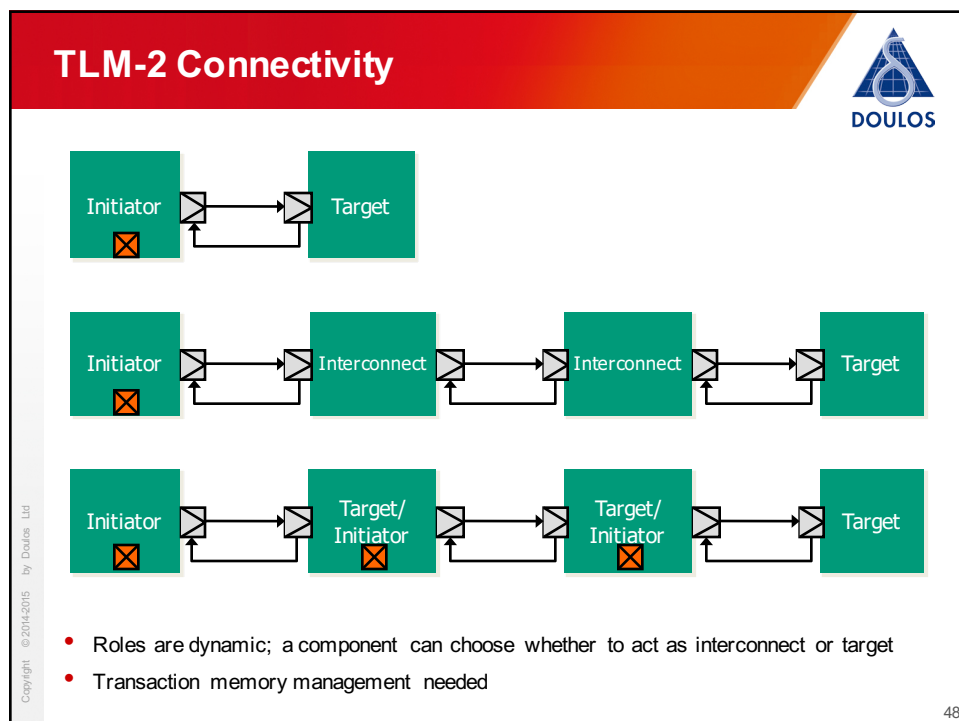


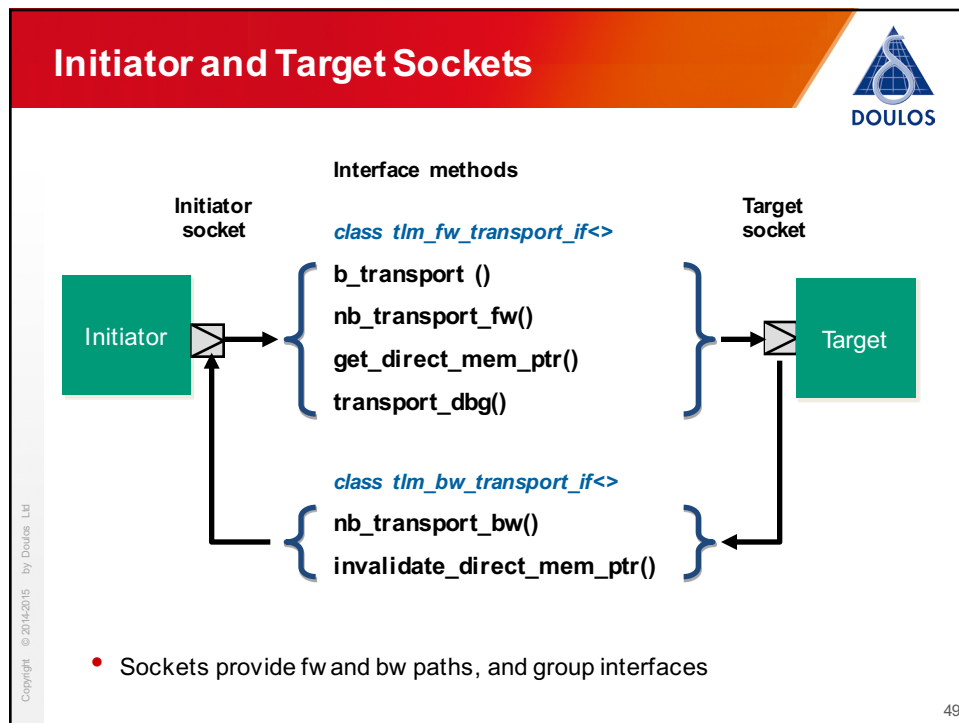
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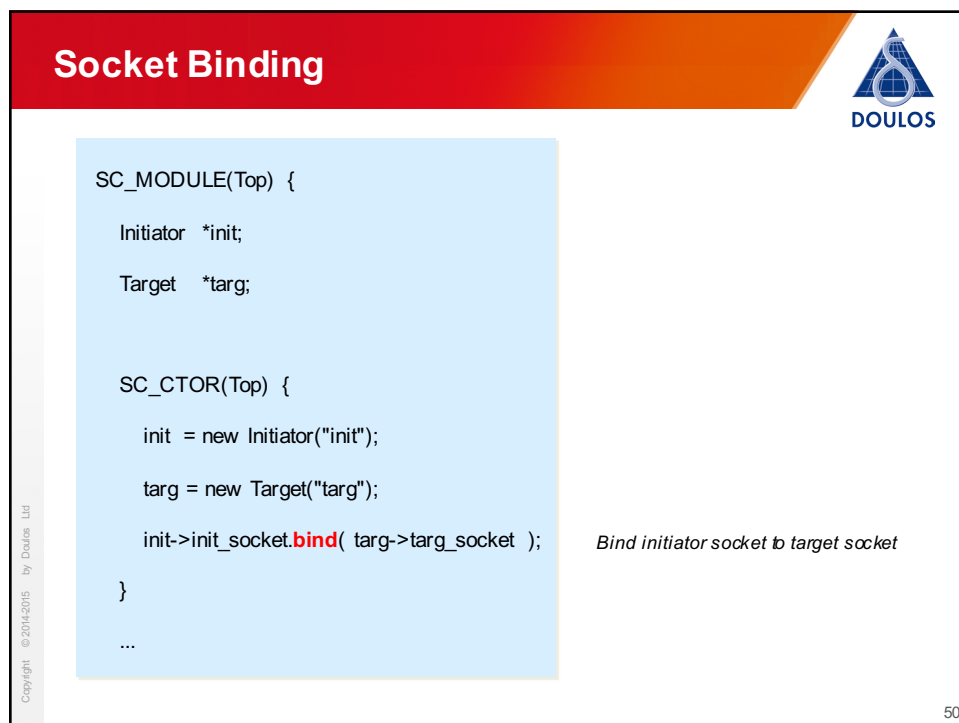


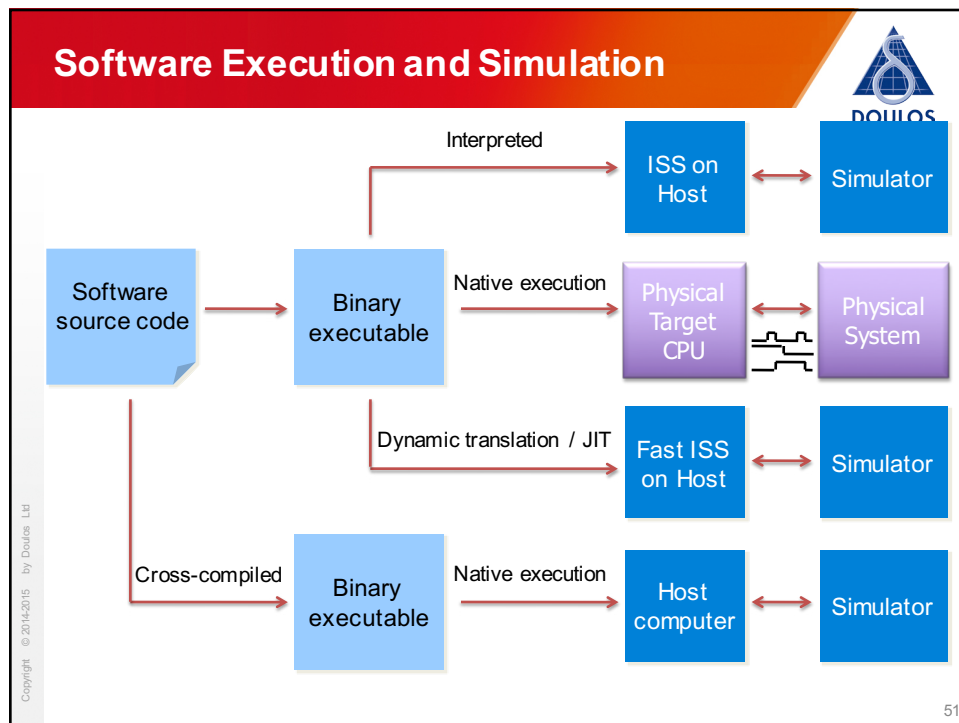
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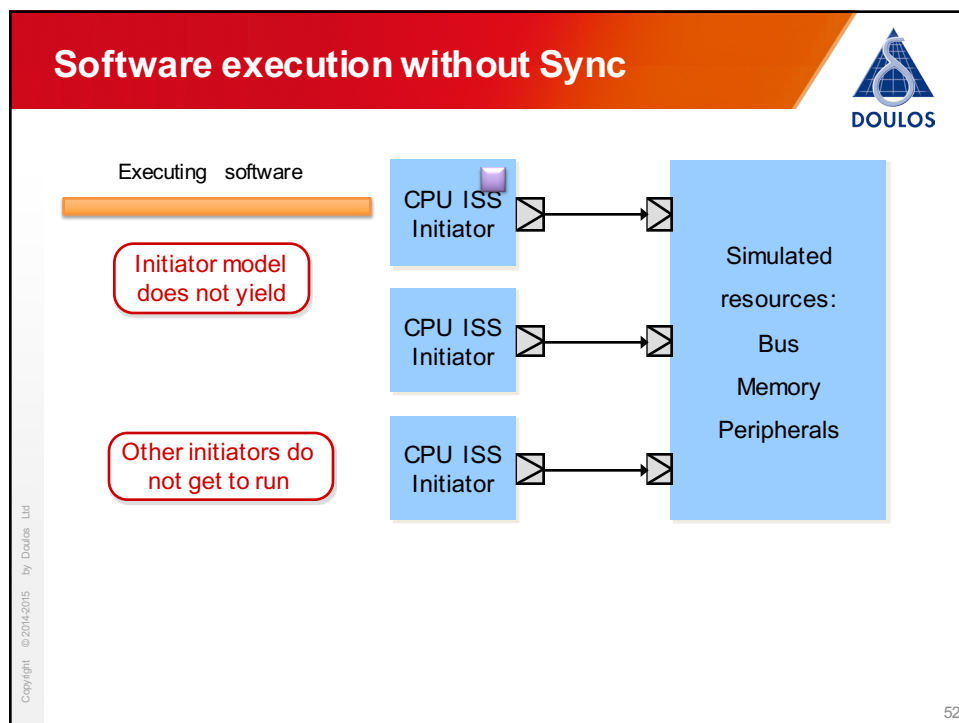


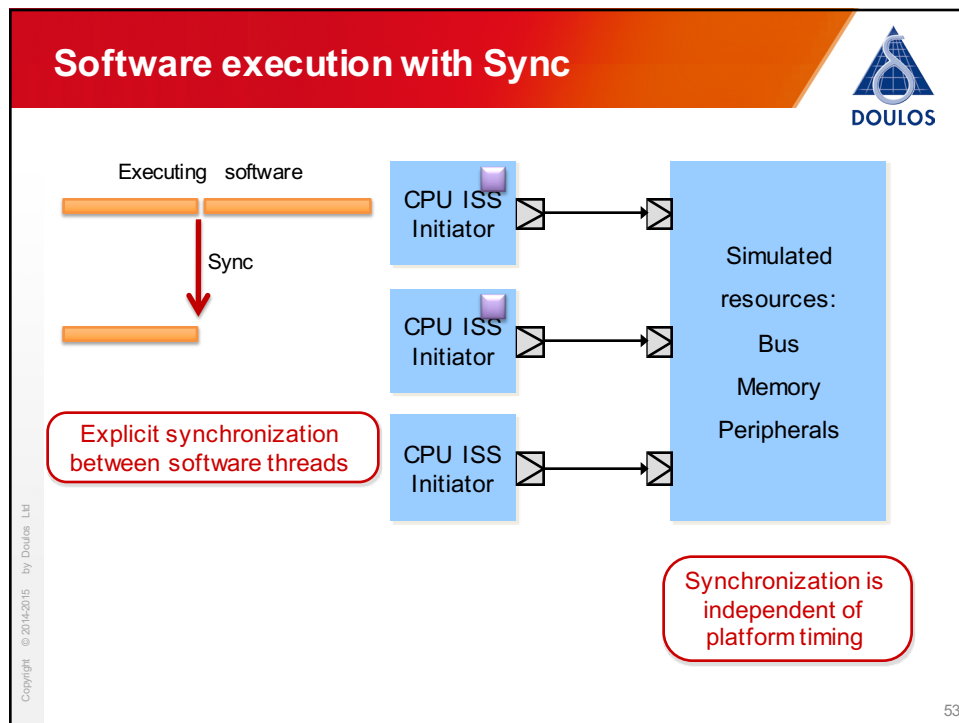
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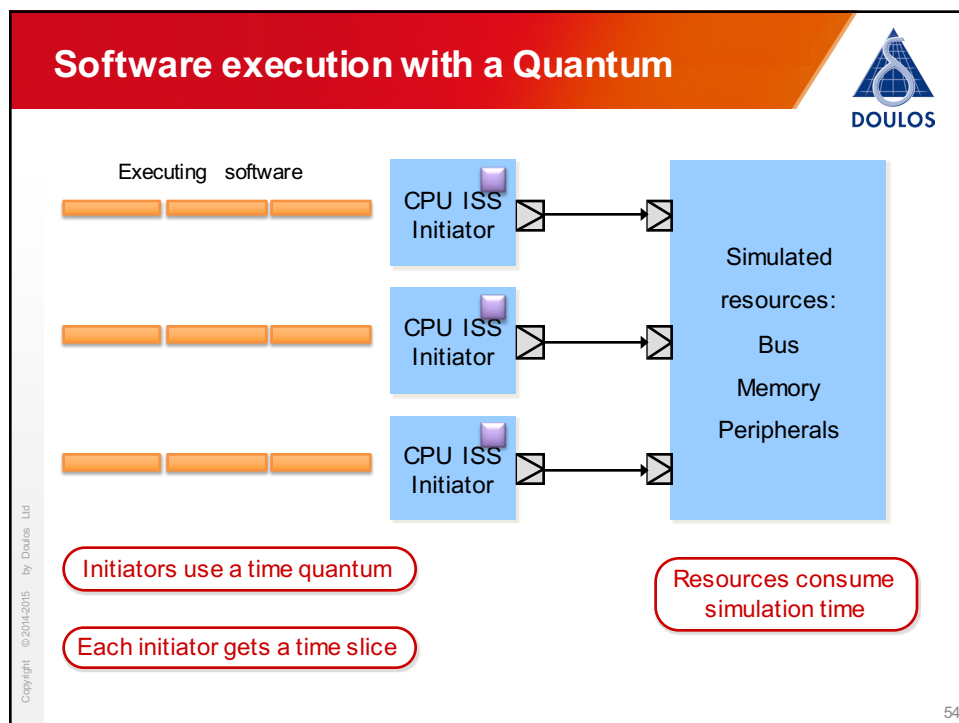


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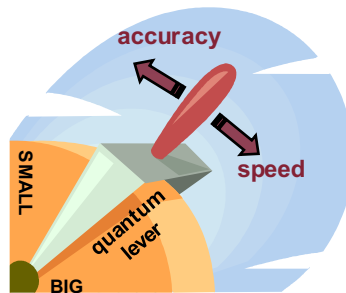
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The Quantum



Quantum can be set by user



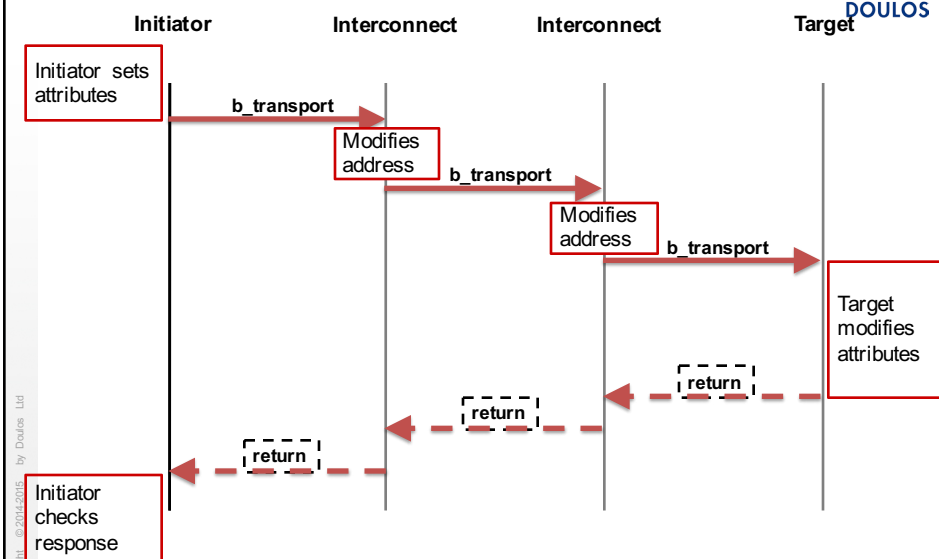
- Typically, all initiators use the same global quantum
- Individual initiators can be permitted to sync more frequently
- Not obliged to use the quantum at all if there are explicit synchronization points
- Quantum could be changed dynamically to “zoom in” (but no explicit support)

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Causality with b_transport



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Timing Annotation and b_transport



```
virtual void b_transport ( TRANS& trans , sc_core::sc_time& delay )
{
    Behave as if method were called at sc_time_stamp() + delay
    ...
    delay = delay + latency;
}
```

```
socket->b_transport( transaction, delay );
```

```
Behave as if method returned at sc_time_stamp() + delay
```

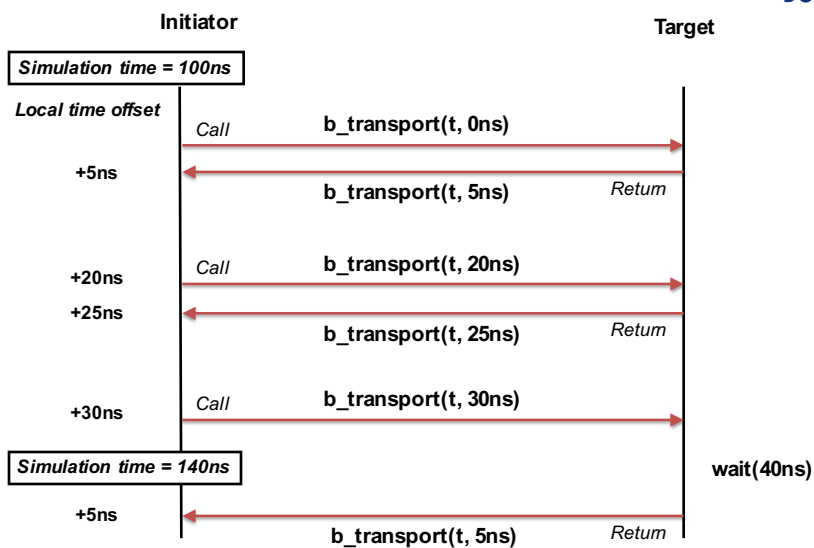
- Recipient may
 - Execute transactions immediately, out-of-order – Loosely-timed
 - Schedule transactions to execute at proper time – Approx-timed
 - Pass on the transaction with the timing annotation

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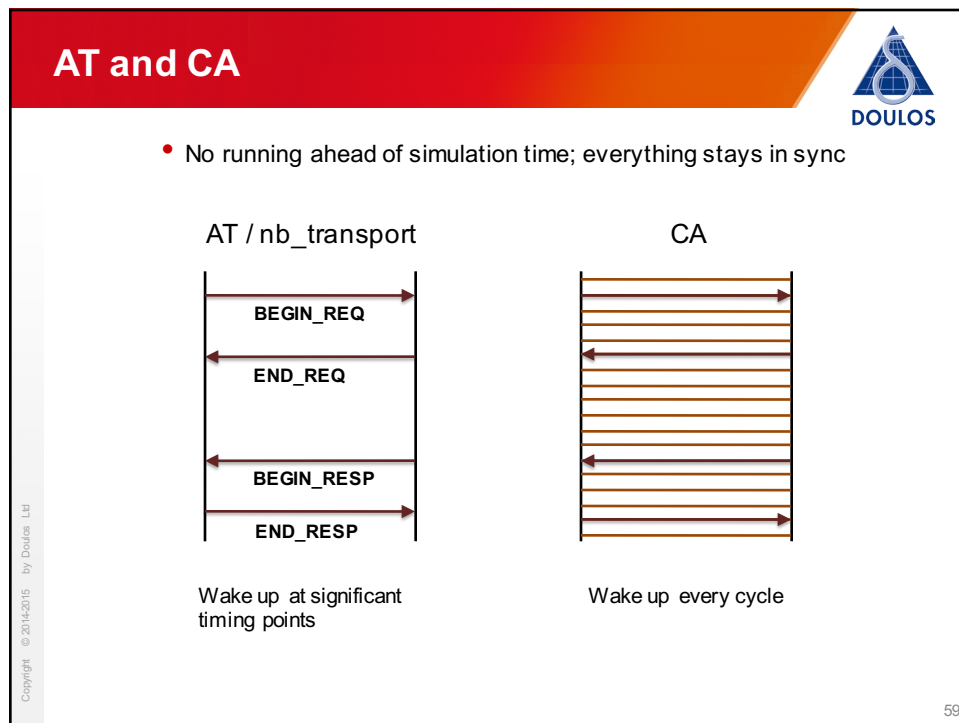
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Temporal Decoupling

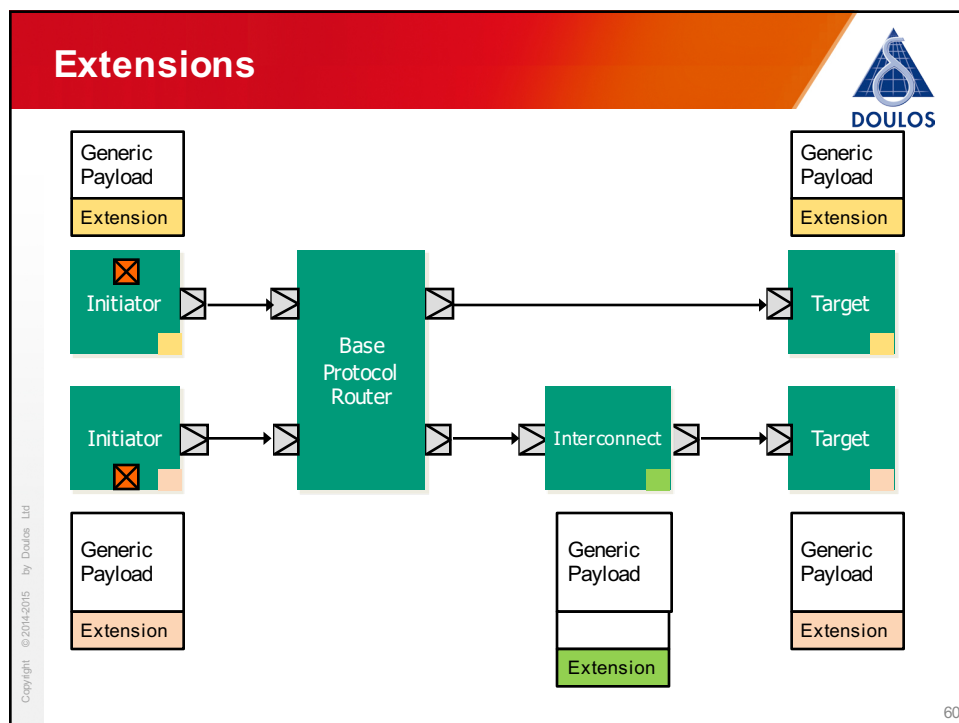


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58



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 - Intel Corporation
 - Mentor Graphics
 - NXP Semiconductors
 - Qualcomm Inc
 - Renesas Mobile
 - ST Microelectronics
 - Synopsys
 - Texas Instruments
- Website <http://www.accellera.org>
- European and North American SystemC Users Groups (and others)
 - <http://www-ti.informatik.uni-tuebingen.de/~systemc>
 - <http://www.nascug.org>

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For More FREE Information



- IEEE 1666

standards.ieee.org/getieee/1666/download/1666-2011.pdf

- ASI SystemC 2.3.1

www.accellera.org

- On-line tutorials

www.doulos.com/knowhow/systemc

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62



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